How to debug a PLL frequency synthesizer

While there are many excellent textbooks on the theory, design and optimization of PLLs, little literature exists to guide a novice in properly debugging the PLL in an engineering lab environment. This article provides some valuable techniques and guidelines in quickly debugging individual portions of a PLL employed in a frequency synthesizer.

By Bob Kelly

Radio systems incorporate frequency synthesizers based on phase lock loop (PLL) technology for various reasons. The benefits of PLLs include:

1) The ease of integration into integrated circuits.

2) The flexibility in the channel spacing for the radio.

3) The high performance available.

4) The small size of the frequency synthesizer.

Many textbooks on the theory, design and optimization of PLLs exist, but there is little literature to guide a novice in properly debugging the PLL in an engineering lab environment.

PLL overview

The simple PLL consists of a frequency reference, a phase detector, a charge pump, a loop filter and a voltage-controlled oscillator (VCO). (Figure 1.) This simple PLL implementation is a fine starting point for creating basic loop equations and understanding the dynamic response. A frequency synthesizer based on PLL technology will add two frequency dividers: one that reduces the reference frequency and one that divides the VCO's frequency. It is also handy to combine the phase detector and charge pump into one block for ease of analysis and a clean

The operation of the PLL is a closed-loop control system, which compares the phase of a reference signal to the phase of the VCO. A frequency synthesizer, with the added reference and feedback dividers, actually compares the two phases scaled by the divider's setting.

diagram. (Figure 2.) These digital divider circuits added to the simple PLL allow easy setting and changing of the operating frequency. A processor will simply "write" a new divider value to a register in the PLL to change the VCO's operating frequency, thereby changing the radio's operating channel.

Description of PLL operation

The operation of the PLL is a closed-loop control system, which compares the phase of a reference signal to the phase of the VCO. A frequency synthesizer, with the added reference and feedback dividers compares the two phases scaled by the divider's setting. This phase comparison is done in the phase detector, which in most systems is a phase and frequency detector. The phase-frequency de-

tector produces an error voltage that is approximately linear over the range of phase errors of $\pm 2*\pi$, and is constant for errors greater in magnitude than $\pm 2*\pi$. (Figure 3.) This dual-mode operation of the phase-frequency comparator produces faster PLL lock times for large frequency errors, such as when the PLL starts at power up, and avoids locking on harmonics.

The VCO creates a frequency based on the control or tuning voltage applied to it. VCOs are available in module form, IC form or can be created from discrete components. Figure 4 depicts a VCO created using active components inside a MAX2361 transmitter IC. The resonant tank and varactors are external, allowing the IF LO to be uniquely defined by the design engineer in support of a particular radio's frequency plan.

The loop filter (Figure 5) integrates the current pulses produced by the phase-frequency detector's charge pump to create the tuning voltage applied to the VCO. Traditionally, the tuning voltage from the loop filter moves higher (more positive) to advance the VCO's phase and to move the VCO to a higher frequency. The loop filter may be implemented with passive components such as resistors and capacitors, or it may employ an operational amplifier. The loop filter time constants, along with the gain of the VCO, phase detector and dividers, sets the PLL bandwidth. The PLL bandwidth then determines the PLL's transient response, reference spurious levels and noise filtering characteristics. At frequencies within the PLL
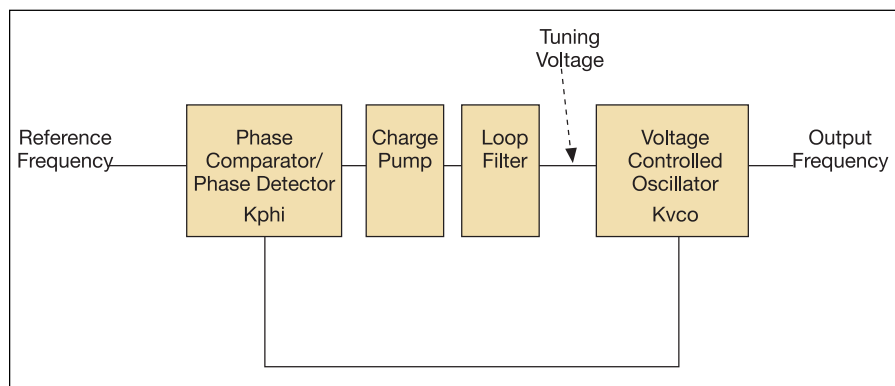

Figure 1. The simple PLL shown in this block diagram produces an output frequency "locked" to the reference.

bandwidth, the phase noise at a synthesizer output is dominated by the phase detector's phase noise. Meanwhile, at frequencies outside of the PLL bandwidth, the output phase noise is due to VCO phase noise.

The frequency synthesizer PLL reference input is a stable, clean constant-frequency signal. In most radios, some form of a crystal oscillator is employed since its phase noise is very low and its frequency is stable and well defined. The PLL will divide this reference to provide a lower frequency for the phase-frequency detector. This lower frequency sets the comparison rate for the detector and establishes the smallest frequency step possible by incrementing the feedback divider by "1." This becomes the frequency resolution of the synthesizer, or frequency step size, which should be equal to or smaller than the channel spacing of the radio system being designed. The phase detector and loop filter create a tuning voltage based on the VCO's output scaled down by the feedback divider. Based on this description, the VCO operating frequency is:

$$F_{VCO} = \frac{F_{REF}}{R} \times N \qquad (1)$$

For example, if the reference frequency (F_{REF}) is 20 MHz, and the reference divider (R) is 2000, a feedback divider setting (N) of 88,103 will produce a VCO frequency (F_{VCO}) as follows:

(20 MHz/2,000) x 88,103 = 881.03 MHz

Changing the feedback divider by 1 to 88,104 produces a VCO frequency of 881.04 MHz, since the comparison frequency is 10 kHz.

This frequency synthesizer multiplies the reference frequency to the UHF band. One byproduct of this PLL multiplication method is the increase in phase noise within the loop's bandwidth. The noise floor of the PLL is increased by 20*log (N) within the loop bandwidth. In the case noted above, the phase noise increased 20*log (88,103) = 98.89 dB. This is why the reference oscillator must be extremely clean. The loop's action will increase the noise floor by ~100 dB, so a clean, high-Q crystal oscillator is mandatory if the output is to be of sufficient quality for modern radio communications.

Please consult existing references for detailed analysis equations.

Bring PLL to life

At this point in your product development cycle, you have read the texts, poured over spreadsheets and simulations, and theoretically obtained every dB of performance possible from your design. Your design is reduced to copper traces on a circuit board.
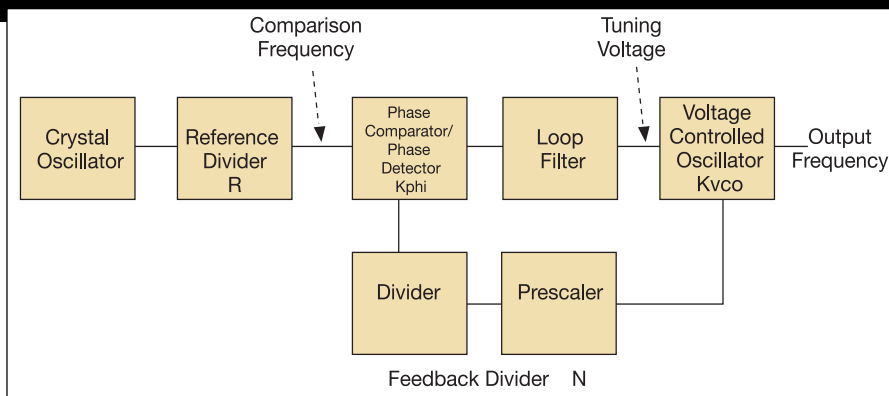

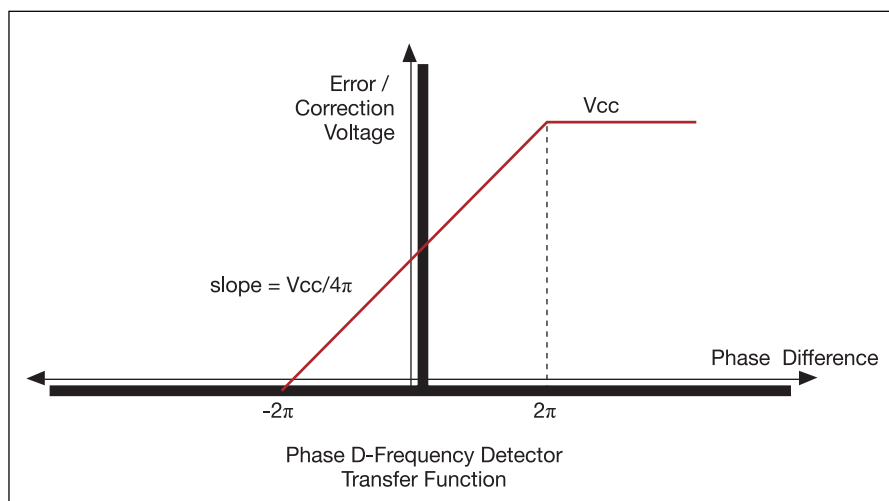**Figure 2. A frequency synthesizer adds digital dividers to a PLL, allowing the output frequency to be programmed.**

Figure 3. The phase-frequency detector produces a control voltage over a ±2π phase range.
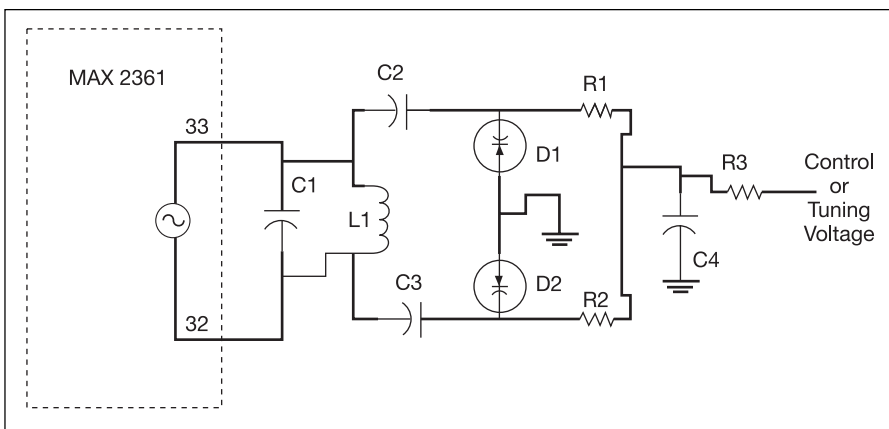

Figure 4. The MAX2361 transmit IC's IF VCO uses external components to set the gain and frequency.

The parts have been installed on the board and the temptation is to rush into the lab, apply power and quickly verify that all your diligent efforts are correct. In a perfect world, this engineering project is on schedule and under budget. Theory and reality are about to meet again, with your design being the conduit between those two disparate domains.

Invest some time to study the PLL's operation before exhaustive performance measurements are begun. Not only must the frequency synthesizer function; it must function properly before data is recorded. Rapid progress is ensured by following a methodical procedure to verify each section of the PLL during your early debugging sessions.

The VCO section

The VCO produces the signal output from a PLL frequency synthesizer, so it determines much of the PLL's performance. If the VCO is not operating properly, many perfor-

mance parameters will be affected. Early in the debug phase, the VCO should be tested to ensure it is providing the intended frequency range, gain and output level. To test the VCO, modify the PLL so that there is no closed-loop control. A common way to "break" the loop is to disconnect R3 (Figure 4) and apply a lab power supply across C4, which allows the VCO tuning voltage to be varied over the desired range. Monitor the VCO's frequency of operation on a frequency counter (or a spectrum analyzer) as the tuning voltage changes. Record the operating frequency at several tuning voltage settings. *Is the VCO at the correct frequency?*

Using data from this simple test will quickly assess if the VCO is able to operate at the desired frequency. If the VCO is to produce an IF LO (intermediate frequency local oscillator) at 183 MHz, and the lowest frequency noted in the test is 187 MHz, it will be impossible for the PLL to lock properly. To correct this condition, verify that all resonant components in the VCO tank are the desired values. For example, if the tank inductor L1 (Figure 4) is too small, the resonant frequency will be shifted up in frequency.

Always keep in mind the equation describing a simple LC tank circuit's resonant frequency:

$$Fres = \frac{1}{2 * \pi * \sqrt{L * C}} \qquad (2)$$

F_{res} is the resonant frequency in Hertz.
L is the inductance in Henries.
C is the capacitance in Farads.
Are the correct parts installed?

Modern reactive components have become so small that visible labels are not possible. This means that components in the VCO are most easily tested by substitution with a known value. Because assembly of the first circuit board may have been completed by hand, it is likely that incorrect values have been soldered on the PCB. Replace tank components as needed to bring the VCO frequency close to the desired operating point (Table 1).

It is possible to correct the VCO's operation as described in Table 1 and the PLL will still exhibit problems. The loop might oscillate if the VCO's tuning gain is not close to the value used when the loop filter components were calculated. In Figure 6, note the slope of the curve described by the lab data from your prototype. The stability of the feedback loop requires the gain of the loop to be in a certain range. If the VCO is on the correct frequency but has a large gain error, the loop itself will oscillate and cause the VCO to be modulated over a broad range of frequencies.

Use your data on the VCO in the open loop condition to verify the loop gain is close to your design-target value. If the VCO tuning gain is too high, the varactors are coupled too tightly to the resonant tank. Confirm that the correct varactors have been installed. The capacitors (C2 and C3 in Figure 4) that couple the varactors to the tank may be too large in value. Conversely, if VCO tuning gain is low, C2 and C3 may need to be increased in value.

The dividers
Can the divider work at the desired frequency?

A PLL design often overlooks the digital frequency divider's specifications. The dividers usually work fine, but a lack of thoroughness on the designer's part will produce a PLL that does not perform as expected. All dividers have a specification for the maximum input frequency (F_{MAX}) and the minimum input level.

In a design that ignores the F_{MAX} specification, the divider will "drop pulses." The closed loop will then detect (in error) that the VCO

is too low in frequency and command the tuning voltage to go still higher. The divider will miss more pulses and the loop will attempt to further push the VCO to a higher frequency. The loop will then enter a "latched" condition where the VCO tuning voltage is held at the positive supply voltage.

The deceptive issue at work is that the feedback divider must not only divide the VCO's expected output, but it must correctly divide the highest frequency that the VCO can produce under locked and unlocked conditions. For the loop to function reliably, transient conditions encountered at start-up or changing channels must not cause feedback polarity reversal.

Is the VCO amplitude sufficient to drive the divider?

The feedback dividers also require a minimum signal amplitude to operate. Ensure that the VCO signal level reaching the divider is well above the data sheet minimum over the entire frequency range of the VCO. Dividers will commonly drop pulses when the signal level is too low, making it impossible for the PLL to obtain stable steady-state operation.

Is the divider programmed with the correct value?

The PLL will not produce the correct frequency if the divider control registers are loaded with the wrong values. It is common to overlook a fixed divide-by-two found in many receiver embedded PLLs, especially in applications with quadrature generation circuits. Last, the PLL control registers may be loaded with the wrong data due to faulty data transmission on the serial bus. Improper data transfer may result from RC networks placed on the serial bus lines to help control noise and interference. Confirm with an oscilloscope that bus timing requirements are met and that valid data are being presented to the pins of the PLL IC.

The loop filter

The loop filter sets the PLL's bandwidth and transient response, and it shapes the PLL's noise spectrum. You can consult textbooks for the relations between loop-filter time constants and these performance behaviors.

Are the correct components installed in the loop filter?

With the wrong parts installed, the bandwidth may be too wide, causing reference frequency spurious sidebands on the PLL output. Or, the bandwidth may be too narrow, causing VCO phase noise to dominate the output spectrum and produce a long settling time. If the damping factor is too low, the loop will oscillate. Polarized filter capacitors have high leakage currents, causing a loop to constantly be correcting with large charge pump pulses. This constant correction causes the reference frequency spurious sidebands to be larger than expected. Install low-leakage capacitors (ceramic, mica or polyester film) to improve this performance.

Is the op-amp in the active filter staying out of saturation?

PLLs with no on-chip charge pump will have phase detector outputs that command a "pump up, pump down" condition. These PLLs will often employ an active loop filter. In the case of an active loop filter, the op-amp's input stages may saturate on each correction pulse from the phase-frequency detector. Recovery from this saturation condition is not well defined or controlled, so the loop dynamics will not be as designed.

The solution is to "split" the op-amp input resistors and place a pole in the filter's response. This will prevent the fast edges from hitting the op-amp input, thereby avoiding pulse-wise saturation. The extra pole must be examined for its impact on loop stability, since it will degrade the design's phase margin.

Also, some op-amp input stages can "change polarity" during power-up conditions, causing the

Table 1. VCO troubleshooting guide suggests common solutions.

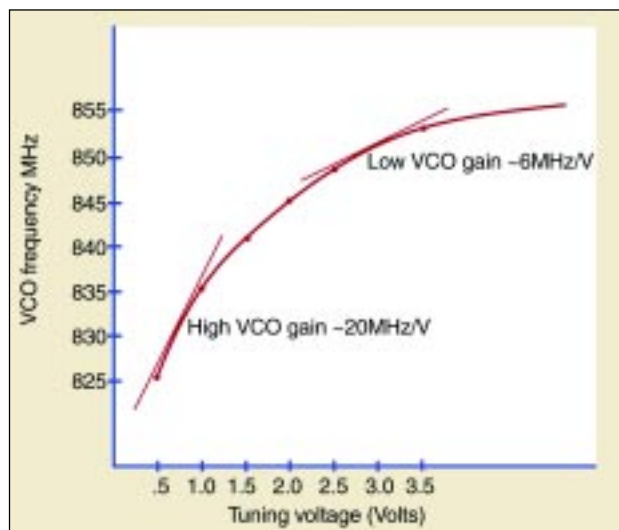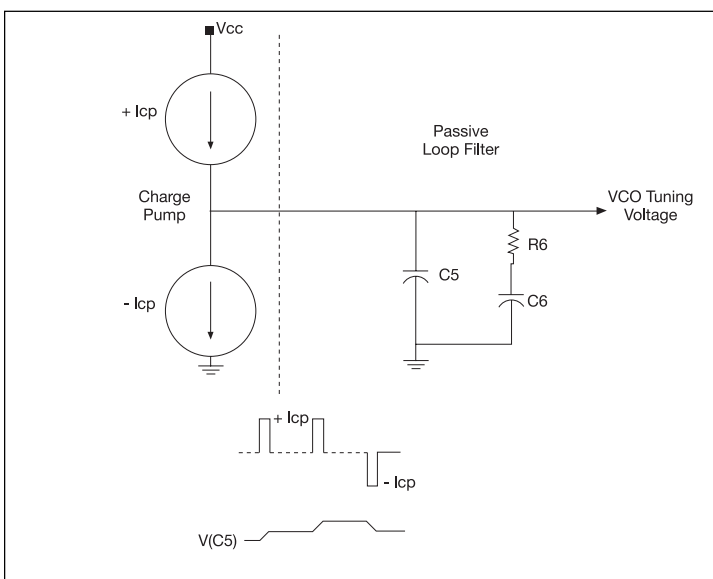| Symptom	Cause	Remedy
VCO frequency too high.	Incorrect tank components.	Replace tank's L & C components with known value parts.
VCO frequency too low.	Incorrect tank components.	Replace tank's L & C components with known value parts.
VCO frequency too low even with correct tank components.	Too much stray capacitance.	New PCB layout in area of VCO, or recalculate tank components with increased stray capacitance values.
No VCO output.	VCO not oscillating.	Confirm varactors are installed with correct polarity. Check solder connections in tank area. Confirm that R1 and R2 are high enough values.
VCO frequency very unsteady.	Marginal design to support oscillation.	Increase VCO's loop gain if possible. Try high Q inductor. Confirm varactor polarity is correct.
VCO frequency very unsteady.	Multiple VCO modes; tuning curve not continuous.	Try lower Q inductor, or decrease R1 and R2. Decrease varactor coupling to tank by lowering C2 and C3. Pick inductor with higher self-resonant frequency.

Figure 6. The VCO tuning-curve data allows the VCO's gain to be computed.

Figure 5. The passive loop filter integrates charge-pump current pulses to produce the VCO tuning voltage (a). Some PLLs use an op-amp in an active loop filter (b).

loop to saturate due to excess positive feedback. The solution is to select an op-amp that is not upset by power-on transient conditions.

The phase-frequency detector and charge pump

The phase-frequency detector and charge pump are usually integrated with other PLL circuits, so if they have been properly designed, there is little room for difficulty. Nevertheless, Mr. Murphy was not copied on the memo that ruled out trouble, so we must expect some room for error.

Phase frequency detectors in most ICs have some aspects of their operation programmed by register values. The polarity of the detector can be set under software control, and the magnitude of the charge pump current may have several user-defined values.

Is the phase detector set for the correct polarity?

Phase detector polarity control allows a PLL IC to function with positive or negative VCO gain, or to account for a signal inversion in an active loop filter. Confirm that the phase detector's polarity is correct to operate with the intended VCO and loop filter. If the loop is latched with the control voltage against the ground or supply rail, a simple bit inversion may be all that is needed to bring life to the PLL.

Is the charge pump current the desired value?

The charge pump is also (often) under user control. This is handy, as it allows a frequency synthesizer to operate over a wide tuning range and correct for the PLL's gain change over the band of interest. This leads to similar loop dynamics and noise character at low, medium and high VCO frequencies. If the charge pump current is not

changed as the synthesizer tunes over its band, the noise sidebands change and the tuning time will vary. If either of these symptoms appear in an otherwise well-behaved PLL, the c h a r g e pump current may be set too low, too high, or is being changed inappropriately for the application.

The printed circuit board

The last aspect of the PLL often considered is the impact of the printed circuit board (PCB). As many RF engineers understand, the PCB is a vital part of the system, and proper design must be observed.

Is the circuit board clean?

The loop filter has already been identified as an area of the PLL that is adversely affected by leakage currents. The leakage due to filter capacitors is improved by using low-leakage capacitors. Another source of leakage is dirt and flux in the area of the filter. Often, a PLL can be improved by using proper cleaning techniques in the area of the filter to remove contamination. Study the PCB under the microscope and confirm that your filter area is free of dirt and flux residue.

Is the VCO tuning line shielded?

A high-gain VCO produces large frequency deviations for small changes in the tuning voltage. The VCO tuning line has high impedance, and noise can easily couple onto the line and modulate the VCO. Digital signals must not be routed near the

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VCO tuning line. Veteran engineers will avoid routing any signals near the VCO tuning just to avoid any impact on the synthesizer's performance. The PLL action does help a bit with this type of noise coupling; low-frequency noise within the loop's bandwidth, is corrected by the loop's excess gain.

Is the VCO shielded?

A VCO acts like a narrow bandpass filter with gain. Any noise with frequency content near the VCO's resonance point will readily couple into the VCO and modulate it. If the VCO tunes over a harmonic of a "strong" crystal oscillator, expect to see spurious outputs if the harmonic energy couples into the VCO tank.

Conclusion

By understanding and evaluating the individual portions of a PLL, the design engineer rapidly brings the frequency synthesizer into operation. Armed with the techniques and information presented here a frequency synthesizer is quickly debugged and the radio system is ready for detailed performance evaluation. **RFD**

References:

1. Ulrich L. Rohde, Digital PLL Frequency Synthesizers: Theory and Design. Prentice-Hall, Englewood Cliff, NJ, 1983.